Claims PTO
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Claims 1-12 cancelled.

13. A semiconductor device having a dielectric layer that comprises:

a first insulating layer, which includes a carbon doped oxide; and

a second insulating layer, formed on the surface of the first insulating layer, that is under compressive stress and that provides superior mechanical strength, when compared to the mechanical strength of the first insulating layer.

14. The semiconductor device of claim 13 further comprising a third insulating layer, which includes a carbon doped oxide, formed on the surface of the second insulating layer.

15. The semiconductor device of claim 14 wherein the first and third insulating layers each consist essentially of a carbon doped oxide, and the second insulating layer comprises a material selected from the group consisting of silicon dioxide, SiOF, silicon nitride, silicon oxynitride, and silicon carbide.

16. The semiconductor device of claim 15 wherein the carbon doped oxide included in both the first and third insulating layers includes between about 5 and about 50 atom % carbon.

17. The semiconductor device of claim 14 wherein the first and third insulating layers are each between about 150 and about 1,500 nanometers thick, and the second insulating layer is between about 2 and about 100 nanometers thick.

18. A semiconductor device having a dielectric layer that comprises:

a first insulating layer, which includes a carbon doped oxide;

a second insulating layer comprising silicon dioxide, which is formed on the surface of the first insulating layer;

a third insulating layer, which includes a carbon doped oxide, that is formed on the surface of the second insulating layer; and

a fourth insulating layer comprising silicon dioxide, which is formed on the surface of the third insulating layer.

19. The method of claim 18 wherein the first and third insulating layers are each between about 150 and about 1,500 nanometers thick and the second and fourth insulating layers are each under compressive stress and are each between about 2 and about 100 nanometers thick.

20. The method of claim 19 wherein the first and third insulating layers each consist essentially of a carbon doped oxide that includes between about 5 and about 50 atom % carbon.

21. A semiconductor device having a dielectric layer that comprises:

a first insulating layer, which has a relatively low dielectric constant and relatively poor mechanical strength, that is between about 150 and about 1,500 nanometers thick;

a second insulating layer, which is formed on the surface of the first insulating layer, that has a relatively high dielectric constant and superior mechanical strength and that is between about 2 and about 100 nanometers thick;

a third insulating layer, which is formed on the surface of the second insulating layer, that has a relatively low dielectric constant and relatively poor mechanical strength and that is between about 150 and about 1,500 nanometers thick; and

a fourth insulating layer, which is formed on the surface of the third insulating layer, that has a relatively high dielectric constant and superior mechanical strength and that is between about 2 and about 100 nanometers thick.

22. The semiconductor device of claim 21 further comprising a dual damascene interconnect, in which a via has been etched through the first, second, third and fourth insulating layers, and in which a trench has been etched through the third and fourth insulating layers.

23. The semiconductor device of claim 22 wherein the second and fourth insulating layers are each under compressive stress.